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1 A Scalable Instruction Buffer and Align Unit for xDSPcore

Panis, C.; Grunbacher, H.; Nurmi, J.;

Solid-State Circuits, IEEE Journal of , Volume: 39 , Issue: 7 , July 2004

Pages:1094 - 1100

[Abstract] [PDF Full-Text (744 KB)] **IEEE JNL** 

2 A fast 7.5 ns access 1K-bit RAM for cache-memory systems

Kawarada, K.; Suzuki, M.; Mukai, H.; Toyoda, K.; Kondo, Y.; Solid-State Circuits, IEEE Journal of , Volume: 13 , Issue: 5 , Oct 1978

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3 280-ps 6-bit RCJL decoder using high drivability and unit circuit for kbit Josephson cache memory

Wada, Y.; Nagasawa, S.; Ishida, I.;

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4 A 32-bit CMOS microprocessor with on-chip cache and TLB

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